

## Article

# Performance of Parallel Connected SiC MOSFETs under Short Circuits Conditions

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**Abstract:** This paper investigates the impact of parameter variation between parallel connected SiC MOSFETs on short circuit (SC) performance. SC tests are performed on parallel connected devices with different switching rates, junction temperatures and threshold voltages ( $V_{TH}$ ). The results show that  $V_{TH}$  variation is the most critical factor affecting reduced robustness of parallel devices under SC. The SC current conducted per device is shown to increase under parallel connection compared to single device measurements.  $V_{TH}$  shift from bias–temperature–instability (BTI) is known to occur in SiC MOSFETs, hence this paper combines BTI and SC tests. The results show that a positive  $V_{GS}$  stress on the gate before the SC measurement reduces the peak SC current by a magnitude that is proportional to  $V_{GS}$  stress time. Repeating the measurements at elevated temperatures reduces the time dependency of the  $V_{TH}$  shift, thereby indicating thermal acceleration of negative charge trapping.  $V_{TH}$  recovery is also observed using SC measurements. Similar measurements are performed on Si IGBTs with no observable impact of  $V_{GS}$  stress on SC measurements. In conclusion, a test methodology for investigating the impact of BTI on SC characteristics is presented along with key results showing the electrothermal dynamics of parallel devices under SC conditions.

**Keywords:** bias temperature instability; SiC MOSFETs; short circuit measurements; threshold voltage shift

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## 1. Introduction

The ability of power devices to withstand short circuit currents is an important reliability metric. SiC MOSFETs, by virtue of a higher critical electric field, can block higher OFF-state voltages with reduced conduction losses while ON. This means SiC MOSFETs usually have smaller die size compared to comparatively rated silicon IGBTs. This smaller die size results in reduced switching losses due to smaller parasitic capacitances. However, this also means higher junction temperatures and smaller short circuit withstand times compared to silicon devices [1]. There are several papers that comprehend the performance and failure mechanisms of SiC MOSFETs under short circuit conditions, such as in [2–4]. In [5], the short circuit withstand time of 1.2 kV SiC MOSFETs was compared to that of 900 V silicon super-junction MOSFETs. The results showed higher performance in the SiC MOSFETs when energy density is used as a metric, however the SiC MOSFETs could not meet the 10  $\mu$ s withstand time, unlike in the silicon devices. In [6], two failure mechanisms were identified in SiC MOSFETs under short circuits, namely, (i) parasitic BJT activation resulting from increased hole current flow in the MOSFET drift region and (ii) thermally induced degradation of the material and interfaces. The simulations showed significantly higher temperatures in the SiC MOSFET due to the smaller die size. In [7], the short circuit performance of 1.2 kV SiC Trench MOSFETs were investigated at low

(400 V) and high (800 V) DC link voltages. The results at high  $V_{DC}$  indicated thermal runaway as the failure mode, while measurements at low  $V_{DC}$  indicated  $V_{GS}$  rupture as the failure mode. NPN BJT activation during short-circuit measurements has also been reported in 3.3 kV SiC MOSFETs [8]. Other studies have also shown that gate oxide failure is a specific failure point in SiC MOSFETs [9–14]. High electric fields and lattice temperature during short circuits can cause gate oxide breakdown due to large leakage currents. In [15], the dependency of the short circuit performance of the SiC MOSFET on the turn-OFF  $V_{GS}$  was investigated and the results showed that turning the device OFF with a higher negative  $V_{GS}$  improved the short circuit performance. This was attributed to higher turn-OFF  $V_{GS}$  suppressing the thermally activated parasitic BJT. It was also shown that increasing the gate oxide thickness of the SiC MOSFET improved the short circuit performance. The failure modes are also described as “fail-to-short” and “fail-to-open” in [16], where a fail-to-open (degradation of the gate structure) is identified as relevant to the application. Different SiC MOSFETs were evaluated, and the gate leakage current was identified as degradation precursor. The gate and drain leakage current during short circuits in SiC MOSFET were also investigated in [17]. The repetitive short-circuit capability of SiC MOSFETs has been evaluated by different authors [18–20].

In [8,21,22] the short circuit performance of 3.3 kV SiC MOSFET was evaluated, whereas 10 kV SiC MOSFETs were investigated in [23,24]. In addition to the new higher voltage rated SiC MOSFETs, the short circuit performance of parallel connected SiC MOSFETs/modules is a highly relevant topic.

The spread of the device characteristics can lead to uneven stresses in multichip structures [16], with results reported in [25] for SiC power modules. In [26] a 1.2 kV/330 A SiC MOSFET module was tested under short circuit conditions with a DC link of 800 V, a peak SC current of 5.4 kA and a withstand time between 2 and 3  $\mu$ s measured. Subsequent failure analysis showed that only some MOSFETs failed, thereby indicating non-uniform stress distribution as the primary cause of module failure. The primary factor was attributed to threshold voltage variation between the parallel connected MOSFETs. Similar results were presented in [27,28], where  $V_{TH}$  mismatch between parallel connected devices was shown to be the cause of failure under short circuit measurements. Parasitic inductance mismatch has also been reported as a cause of short circuit current failure in parallel connected SiC MOSFETs [13].

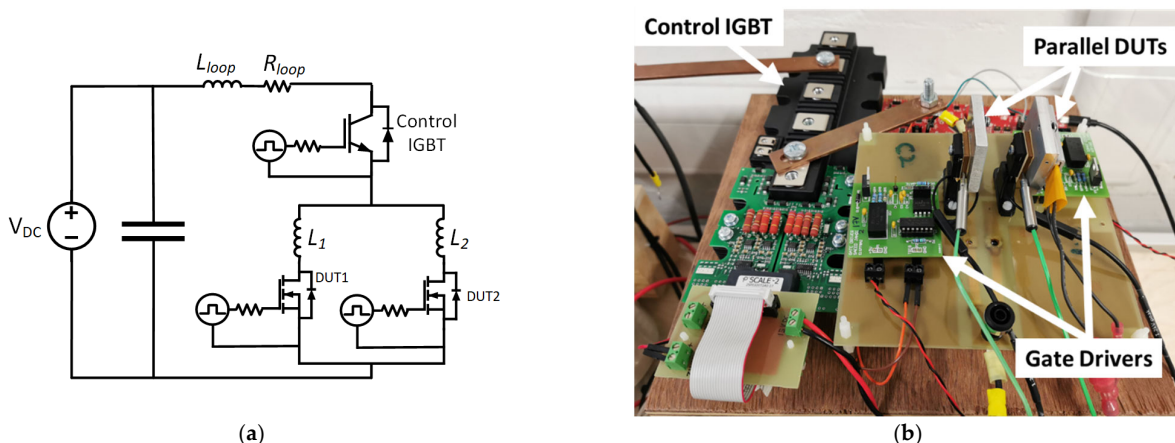
This paper contributes to the study of short circuits in parallel connected SiC MOSFETs by investigating the relative impacts of mismatch in (i) threshold voltage, (ii) MOSFET switching rate, and (iii) initial junction temperature. This was investigated for both planar and trench MOSFETs from three different device manufacturers. Threshold voltage shift from bias temperature instability is known to be an important phenomenon in SiC MOSFETs [29–31]. In this paper, a new test methodology that combines both BTI and short circuit tests is introduced. Section II describes the test setup and presents the experimental results. Section III introduces the experimental methodology for evaluating the role of BTI in the short circuit characteristics. Section IV complements the experimental results with modeling of short circuits in SiC MOSFETs, and Section V concludes the paper.

## 2. Experimental Measurements for Short Circuits

The experimental test rig circuit diagram is shown in Figure 1a, and the experimental circuit picture is shown in Figure 1b. In Figure 1a,  $L_{loop}$  is the total loop inductance,  $R_{loop}$  is the total loop resistance,  $L_1$  and  $L_2$  are the lumped total series parasitic inductance (internal device inductances plus PCB track inductance) of the parallel devices, and  $V_{DC}$  is the supply voltage.

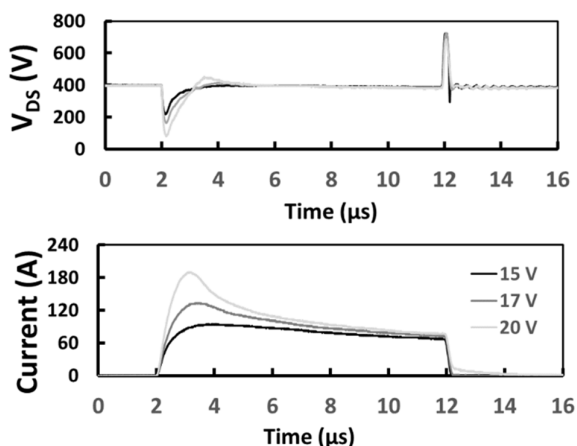
The test-rig comprises a DC power source, a 90  $\mu$ F capacitor bank, a 1.2 kV/1 kA control IGBT module with datasheet reference FF1000R17IE4 and the devices under test (DUTs). Various of DUTs are tested including 1.2 kV planar MOSFETs, 1.2 kV SiC Trench MOSFETs, 650 V SiC Trench MOSFETs and 1.7 kV SiC Planar MOSFETs. Rogowski coils

are used for current measurements and differential voltage probes are used for voltage measurements.



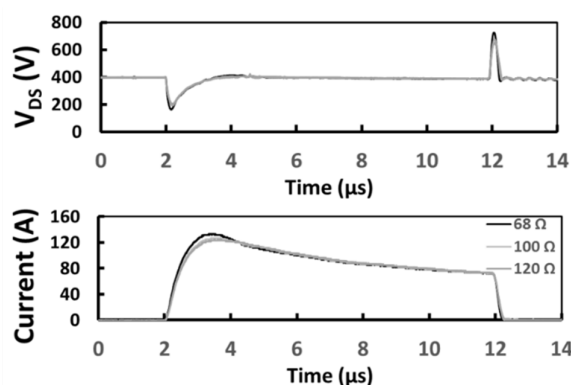
**Figure 1.** Experiment setup: (a) experimental test-rig circuit diagram for short circuit measurements; (b) experimental test-rig picture.

Figure 2 shows the measured voltage and current waveforms from the short circuit measurements for a single DUT (1.2 kV SiC planar MOSFET) driven with  $V_{GS} = 15$  V, 17 V and 20 V. The peak short circuit current increases with increased  $V_{GS}$  due to reduced channel resistance. The negative and positive  $V_{DS}$  spike at turn-ON and turn-OFF is due to the voltage drop across the parasitic inductance subtracting and adding to the device  $V_{DS}$  voltage. The longer short circuit withstand times are due to the lower  $V_{DS}$  of the measurements, which is a third of the device rating.



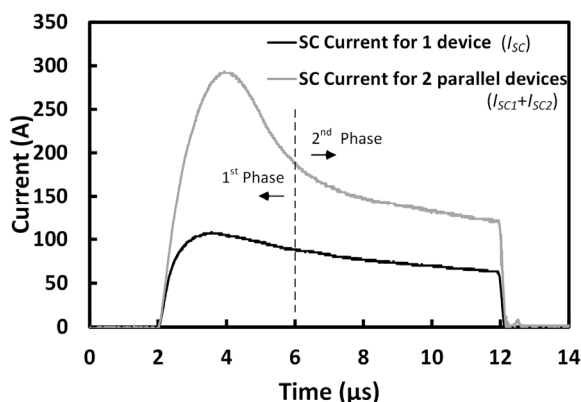
**Figure 2.** Short circuit measurements for  $V_{DS}$  and current in SiC MOSFET with  $V_{GS} = 15$  V, 17 V and 20 V.

Figure 3 shows short circuit measurements for a 1.2 kV SiC Planar MOSFET with three different gate resistances, namely,  $R_G = 68 \Omega$ ,  $100 \Omega$  and  $120 \Omega$ . The measurements show that the peak short circuit current increases marginally with reduced  $R_G$ .



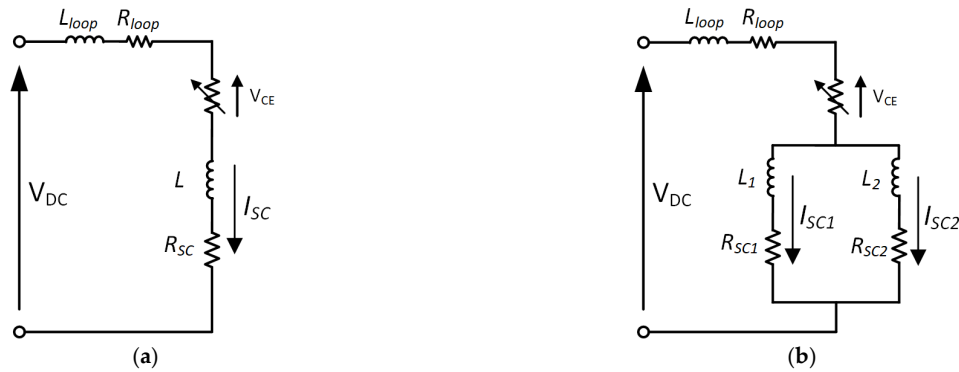
**Figure 3.** Short circuit measurements for  $V_{DS}$  and current in SiC MOSFET with  $R_G = 68, 100$  and  $120 \Omega$ .

As devices are paralleled, it is expected that the total peak short circuit current increases due to the reduced SC resistance of the parallel pair. Figure 4 shows the measured SC currents for a single SiC MOSFET and a parallel pair. It can be observed that although the final SC current in the parallel devices is twice that of the single device, the peak SC current is approximately three times. This difference is due to the fact the SC currents have two phases. The first phase is limited by the series inductance and if affected by the threshold voltage, gate resistance and switching speed of the device. The second phase of the SC current is limited by the temperature coefficient of the short circuit resistance ( $R_{SC}$ ).



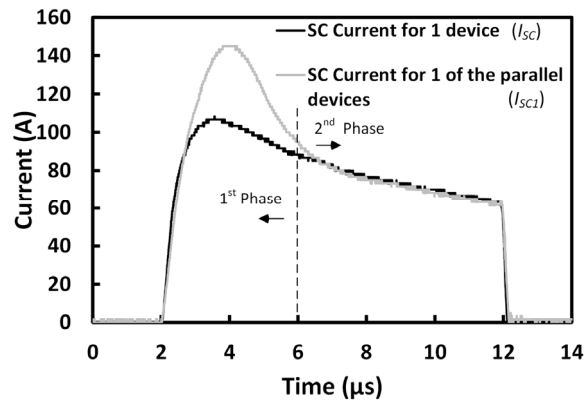
**Figure 4.** Measurements of SC current for a single SiC MOSFET and 2 parallel SiC MOSFETs.

The trebling of the peak SC current is due to the paralleling of the device parasitic inductances. Hence, as devices are placed in parallel, the total SC current increases by more than a factor of the number of devices. Therefore, as the number of parallel devices is increased, the SC current per device increases, with the potential of leading to over-currents. This can be quantified considering the circuits in Figure 5a, which shows the equivalent circuit of the SC measurement of a single device ( $I_{sc}$ ), and Figure 5b, which shows the equivalent circuit for two parallel devices with SC currents  $I_{sc1}$  and  $I_{sc2}$ . Figure 5a,b also shows the voltage drops in the series IGBT as well as the DC link parasitic inductance and resistance.



**Figure 5.** Equivalent circuit of devices under test: (a) single device under short circuit; (b) parallel-connected devices under short circuit.

Figure 6 shows the comparison of  $I_{SC}$  and  $I_{SC1}$ . It can be seen from Figure 6 that during the first phase of the SC current, the peak SC current per device increases in the parallel devices compared to the single device ( $I_{SC1}$  is 37% greater  $I_{SC}$ ). However, in the second phase of the SC, the role of the parasitic inductance is minimized; hence, the SC current per device is independent of the number of parallel devices.



**Figure 6.** Measurement of the short circuit currents through a 650 V SiC Trench MOSFET under single device short circuit condition and under parallel short circuit condition.

A key parameter in determining the impact of paralleling on the total SC current is the series parasitic inductance of the DC link. This DC link inductance will determine the difference between the peak currents  $I_{SC}$  and  $I_{SC1}$  shown in Figure 6. The following model explains the role of this inductance.

From the equivalent circuit in Figure 5a, the SC current for a single device is given by Equation (1) below:

$$i_{SC} = \frac{V_{DC} - V_{CE}}{L + L_{loop}} \cdot \frac{1}{s + \frac{R_{loop} + R_{SC}}{L + L_{loop}}} \quad (1)$$

where  $V_{CE}$  is the IGBT forward voltage,  $L$  is the lumped series parasitic inductance and  $R_{SC}$  is the short circuit resistance of the single SiC MOSFET.

For parallel devices, as shown in Figure 5b, the peak short circuit current is given by

$$i_{SC} = \frac{V_{DC}}{(R_{loop} + sL_{loop})} \left( \frac{\frac{1}{R_{SC1} + sL_1} + \frac{1}{R_{SC2} + sL_2}}{\frac{1}{R_{loop} + sL_{loop}} + \frac{1}{R_{SC1} + sL_1} + \frac{1}{R_{SC2} + sL_2}} \right) \quad (2)$$

$$i_{SC} = V_{DC} \frac{As + B}{s^2 + Cs + D}$$

where

$$A = \frac{L_1 + L_2}{L_1 L_2 + L_1 L_{loop} + L_2 L_{loop}}$$

$$B = \frac{R_{SC1} + R_{SC2}}{L_1 L_2 + L_1 L_{DC} + L_2 L_{loop}}$$

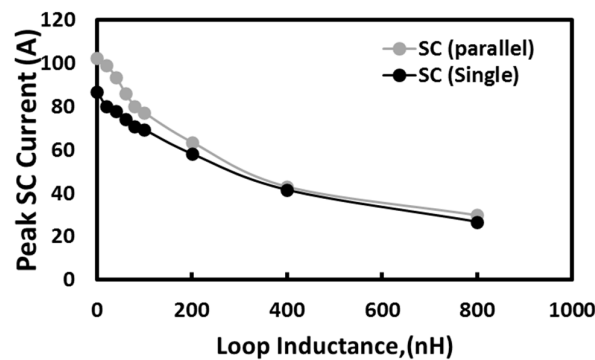
$$C = \frac{L_1 R_{loop} + L_2 R_{loop} + L_1 R_{SC2} + L_2 R_{SC1} + L_c R_{SC1} + L_{loop} R_{SC2}}{L_1 L_2 + L_1 L_c + L_2 L_{loop}}$$

$$D = \frac{R_{loop} R_{SC1} + R_{loop} R_{SC2} + R_{SC1} R_{SC2}}{L_1 L_2 + L_1 L_{loop} + L_2 L_{loop}}$$

The parasitic inductance can be calculated by using the equation below. In the equation,  $V_{overshoot}$  is measured as overshoot voltage during the turn-OFF of the short-circuit as shown in Figure 2. This overshoot voltage is due to the total parasitic inductance, including the device drain inductance and parasitic inductance in series with the device.

$$L_1 + L_{loop} = \frac{V_{overshoot}}{di_{SC}/dt} = \frac{323}{330 \times 10^6} = 0.97 \mu H$$

Assuming  $L_1 = L_2 = 50$  nH (estimated parasitic source and drain inductances of a TO-247 package and PCB track),  $R_{loop} = 0.1 \Omega$ ,  $R_{SC1} = R_{SC2} = 3.5 \Omega$  (derived as average resistance taken from measurements) and  $V_{DC} = 400V$ , Equation (2) can be solved to show the impact of  $L_{DC}$  on the SC current per device under parallel connection. Since the IGBT forward voltage ( $V_{CE}$ ) is significantly smaller than the supply voltage ( $V_{DC}$ ), this does not impact the SC currents. Figure 7 compares the calculated peak SC current for a single device and a device under parallel connection as a function of the busbar inductance. It can be seen from Figure 7 that the difference in the peak SC current between the single device and the single-device in parallel increases as the bus-bar inductance reduces. Hence, in applications that use power modules in circuits with low busbar inductance, the SC per device can be much higher than expected from a single device.



**Figure 7.** Calculated peak SC current for single and parallel MOSFET as a function of total loop inductance.

Measurements on parallel connected SiC MOSFETs with differences in  $V_{TH}$ ,  $R_G$  and initial junction temperature have been performed. Differences in  $V_{TH}$  can arise from variability in the manufacturing process and when that is minimized by careful pre-screening,  $V_{TH}$  drift from BTI can cause  $V_{TH}$  variation between parallel connected devices over the life of the power module. BTI is the process by which positive  $V_{GS}$  stress causes  $V_{TH}$  to increase due to negative charge trapping, and negative  $V_{GS}$  stress causes  $V_{TH}$  to decrease due to

positive charge trapping. The higher interface and fixed oxide charges in SiC (due to the presence of carbon atoms during the gate oxidation process in the fabrication flow) is responsible for the more active nature of BTI in SiC MOSFETs. The random nature of trapped charge occurrence means that devices can exhibit varying degrees of  $V_{TH}$  shift under identical conditions.

For SiC MOSFETs from different manufacturers, the threshold voltage distribution has been measured on a batch of devices. The threshold voltage was measured by shorting the drain to the gate, forcing 10 mA through the channel and measuring the  $V_{DS}$  as described in [32]. Figure 8 shows the measured  $V_{TH}$  distribution on devices from different manufacturers. The results show a wide range and standard deviation of  $V_{TH}$  in SiC MOSFETs, hence emphasizing why it is important to analyze short circuit performance of parallel devices.

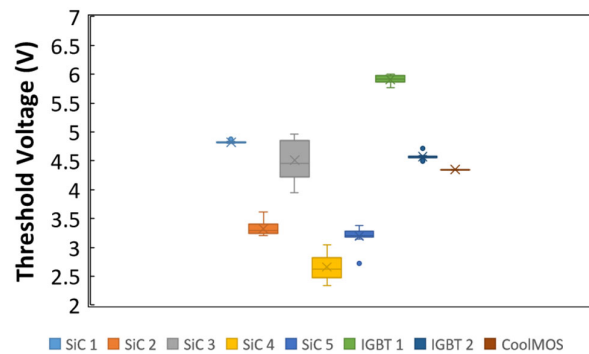
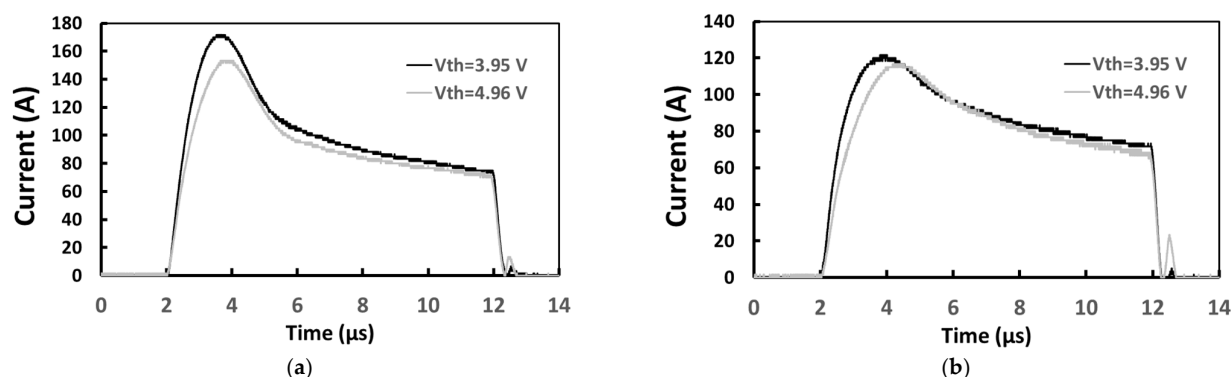


Figure 8.  $V_{TH}$  distribution on devices from different manufacturers.

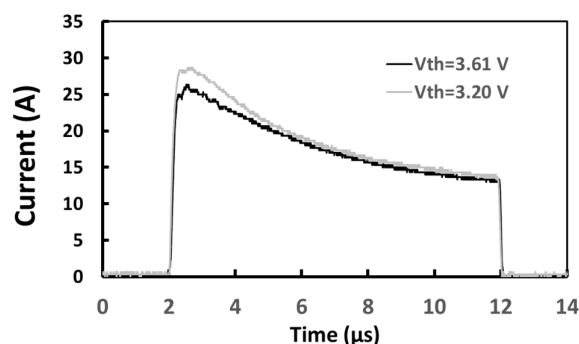
Figure 9a shows short circuit measurements on parallel connected 1.2 kV SiC Planar MOSFETs with 25% difference in  $V_{TH}$  and  $V_{GS} = 17$  V, while Figure 9b shows similar measurements on the same device with  $V_{GS} = 15$  V. The measurements in Figure 9 show that a 25% difference in  $V_{TH}$  leads to a 12.5% difference in the peak short circuit current at  $V_{GS} = 17$  V and 5% difference at  $V_{GS} = 15$  V. The device with the lower  $V_{TH}$  has a higher peak SC current due to the reduced channel resistance according to Equation (3).

$$R_{DS(on)} = \frac{L_{ch}}{W\mu C_{ox}(V_{GS} - V_{TH})} + \frac{L_{drift}}{q\mu N_D A} \quad (3)$$

Similar measurements were performed on parallel connected 1.7 kV SiC MOSFET from another manufacturer and with a  $V_{TH}$  difference of 12.8%. Figure 10 shows the short circuit measurement results, where the device with the lower  $V_{TH}$  is shown to conduct 10% higher peak current. As the device voltage rating is increased, the short circuit current reduces due to higher ON-state resistance. The impact of  $V_{TH}$  mismatch is apparent at both 1.2 and 1.7 kV voltage ratings. The main impact of the  $V_{TH}$  mismatch is in the peak SC current. At the end of the SC pulse, the currents in both devices converge.



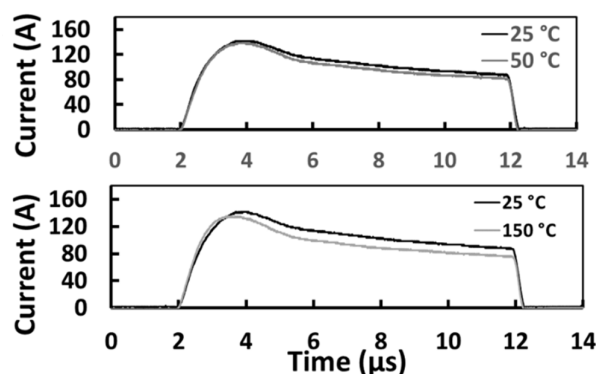
**Figure 9.** Measured short circuit current for parallel 1.2 kV/20 A SiC MOSFETs with 25% difference in  $V_{th}$ : (a)  $V_{GS} = 17$  V; (b)  $V_{GS} = 15$  V.



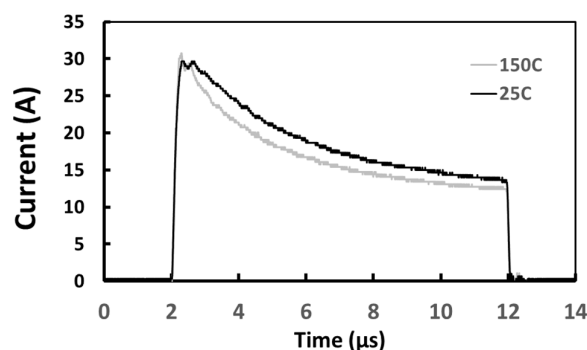
**Figure 10.** Measured short circuit current for parallel 1.7 kV/5 A SiC MOSFETs with 12.8% difference in  $V_{th}$ .

Measurements were performed on parallel devices set with different initial junction temperatures. Figure 11 shows the results of the SC measurements on the parallel connected 1.2 kV MOSFETs set with 100% and 500% difference in initial junction temperature. Initial junction temperature difference is important to consider because power devices on the same substrate can experience different rates of thermo-mechanical degradation. These differences in thermo-mechanical degradation rates can cause differences in the junction-to-case transient thermal impedance and hence differences in the junction temperature. The results in Figure 11 show that  $T_j$  mismatch in parallel connected devices has a marginal impact on the peak SC current unlike  $V_{th}$  mismatch where there is a more prominent difference in the peak SC current. Unlike the measurements in Figures 9 and 10 corresponding with the  $V_{th}$  mismatch, the currents in Figure 11 do not converge over the SC duration. Figure 11 shows that a 100% difference in  $T_j$  leads to a 6.1% difference in the SC energy, while a 500% difference in  $T_j$  leads to a 12% difference in the SC energy with the higher  $T_j$  device dissipating less energy due to the higher temperature coefficient of the saturation resistance. Figure 12 shows similar measurements for parallel connected 1.7 kV SiC MOSFETs set with 500% difference in initial  $T_j$ .





**Figure 11.** Measured short circuit current for parallel 1.2 kV/20 A SiC MOSFETs with 100% and 500% difference in  $T_j$ .



**Figure 12.** Measured short circuit current for parallel 1.7 kV/5 A SiC MOSFETs with different junction temperatures.

The impact of differences in the MOSFET switching rate (controlled by  $R_G$ ) on current sharing under SC have also been analyzed. Over the operational life of the module, degradation in the gate wirebond can cause reduced switching rates in power devices due to increased gate current path impedance. Hence, it is possible that a power module undergoes a short circuit event with parallel devices that switch at different rates as a result of different degrees of gate wirebond degradation. Figure 13 shows the SC measurements on parallel connected 1.2 kV SiC MOSFETs with 20% and 370% difference in  $R_G$ . A 20% difference in  $R_G$  does not cause any difference in the SC characteristics, whereas a 370% difference in  $R_G$  causes a 5.7% difference in the SC energy with the faster switching device dissipating more SC Energy. Because a 370% difference in  $R_G$  is high and is indicative of significant reliability problems, it can be concluded that small and moderate differences in  $R_G$  do not impact the performance of the module under SC conditions.

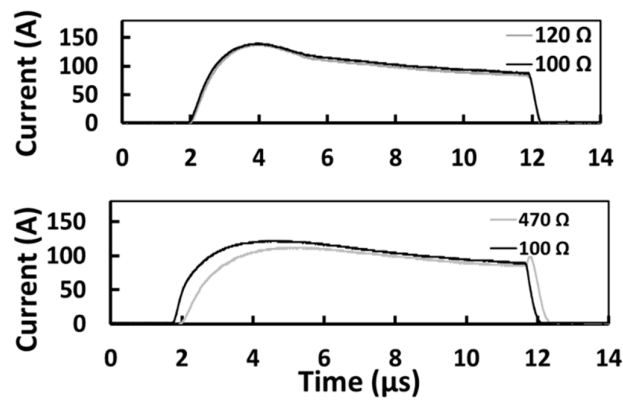


Figure 13. Measured short circuit current for parallel 1.2 kV/20 A SiC MOSFETs with 20% and 370% difference in  $R_G$ .

### 3. BTI and SC Measurements

In this section, the impact of threshold voltage shift ( $\Delta V_{TH}$ ) from BTI on short circuit characteristics of SiC MOSFETs were investigated. In SiC MOSFETs, biasing the gate terminal is known to cause a threshold voltage shift [33], which depends on the magnitude and duration of the bias stress. This  $\Delta V_{TH}$  can have implications on the SC performance of SiC MOSFETs, and this has been experimentally characterized in this section. The experiment is performed by applying a pre-stress  $V_{GS}$  pulse on the gate of the SiC device before testing the DUT under short circuit conditions. The pulse sequence is shown in Figure 14, where the control IGBT gate pulse and the DUT pulse is shown.

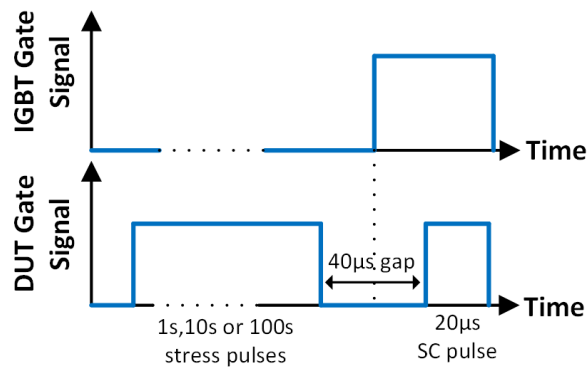


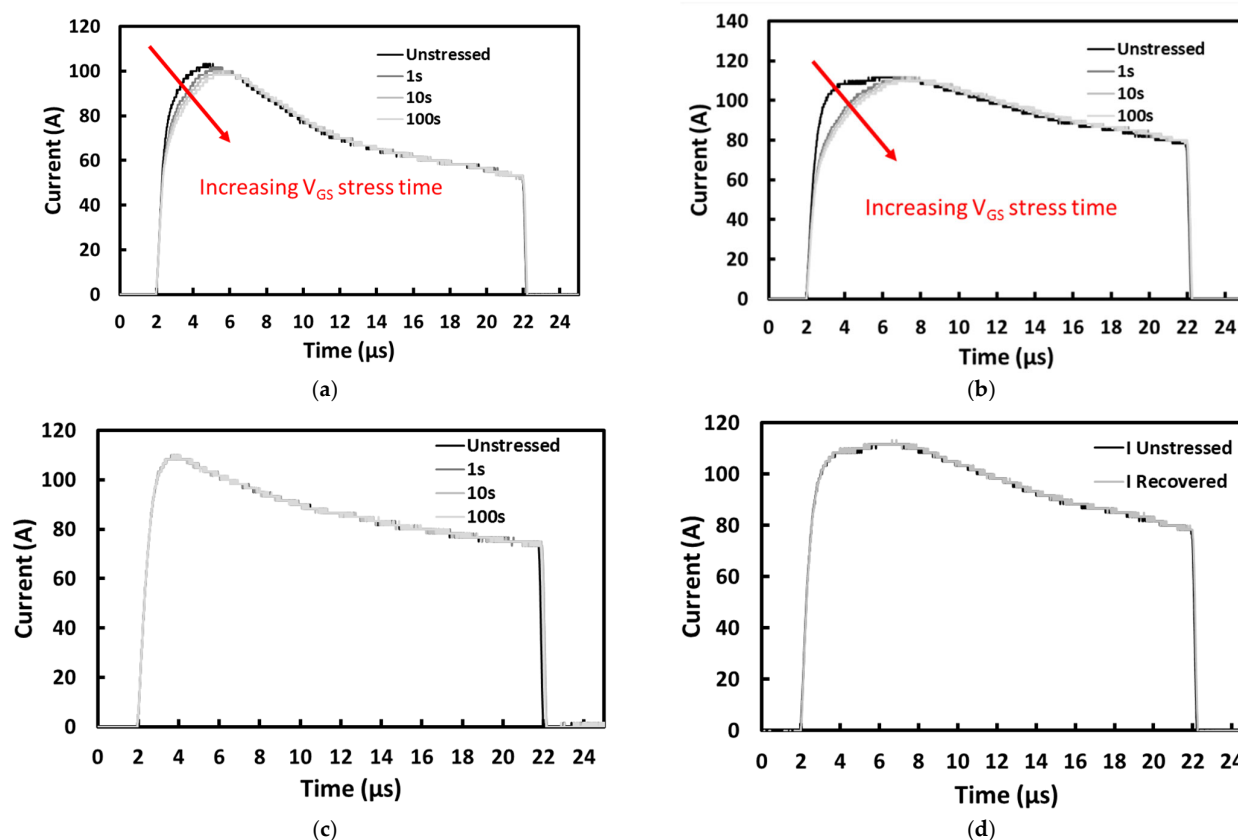
Figure 14. Gate pulse signals for the IGBT and DUT for BTI and SC tests.

The short-circuit tests (duration of 20  $\mu$ s at a DC link voltage of 200 V) is performed 40  $\mu$ s after stress removal, thereby minimizing the impact of the recovery time on the measured SC current. A time of 40  $\mu$ s was chosen to allow sufficient time for the IGBT to turn-ON while also capturing the influence of trapped charges on the short circuit performance since  $V_{TH}$  recovery from the release of trapped charges can affect the measurements. This recovery after stress removal is one of the main challenges of BTI characterization in SiC MOSFETs [20–22]. The duration of the pre-test  $V_{GS}$  stress pulse is varied as to investigate the impact of pulse duration on the SC characteristics. The selected value of  $V_{GS}$  for stress and the SC evaluation is 17 V.

The results of the test described in Figure 14 are shown in Figure 15a for the 1.2 kV SiC Trench MOSFET, Figure 15b for the 1.2 kV SiC Planar MOSFET and Figure 15c for a silicon IGBT device. All the measurements in Figure 15 have been performed at a case temperature of 25  $^{\circ}$ C. The results for the SiC MOSFETs in Figure 15a,b show a slightly reduced short circuit charge as the  $V_{GS}$  stress duration increases from 1 s to 100 s. The

application of the pre-test  $V_{GS}$  voltage causes a rise in  $V_{TH}$  due to negative charge trapping [34], which subsequently causes a reduction in the short circuit current. Similar measurements performed on a 650 V silicon IGBT are shown in Figure 15c. It is apparent that the SC characteristics of the IGBT remain invariant of pre-test  $V_{GS}$  stress pulses. The results in Figure 15 indicate that while BTI impacts the SC characteristics of SiC devices, it has no impact on silicon IGBTs.

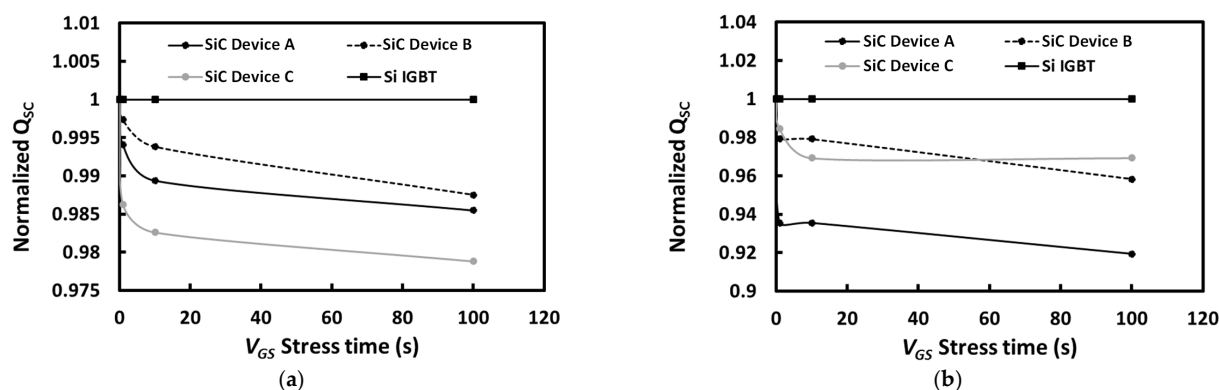
After sufficient recovery time, the  $V_{TH}$  of the stressed device reverts back to its pre-stressed value since all the trapped negative charges are subsequently released. Figure 15d shows the SC measurements of the fully recovered device where the recovery time was 15 min. It can be seen from Figure 15d that the SC characteristics are identical to that measured in the unstressed device; hence, the  $V_{TH}$  has recovered fully to the pre-stress value.



**Figure 15.** Impact of BTI on SC currents for devices: (a) 1.2 kV SiC Trench MOSFET; (b) 1.2 kV SiC Planar MOSFET; (c) 650 V Silicon IGBT; (d) SC measurements performed on fully recovered SiC Planar MOSFET showing  $V_{TH}$  is restored to its pre-test value.

The short circuit current was integrated over time to yield the SC charge. Figure 16a shows the normalized short circuit charge for 3 SiC MOSFETs and 1 silicon IGBT after undergoing a combination of BTI and SC tests. The reduction in the SC charge after BTI stress is apparent for the SiC MOSFETs but not in the silicon IGBT. The reduction in SC charge ranges between 5% and 25% for the SiC MOSFETs. At face value, a reduction in SC charge/current due to an increase in  $V_{TH}$  (from negative charge trapping) may not be negative consequences since the SC energy is reduced for the device; however, this can have a significant impact on the reliability of parallel connected SiC MOSFETs under SC conditions. Non-uniform current sharing of SiC MOSFETs under SC conditions has been cited as the primary cause of power module failure under SCs [16].

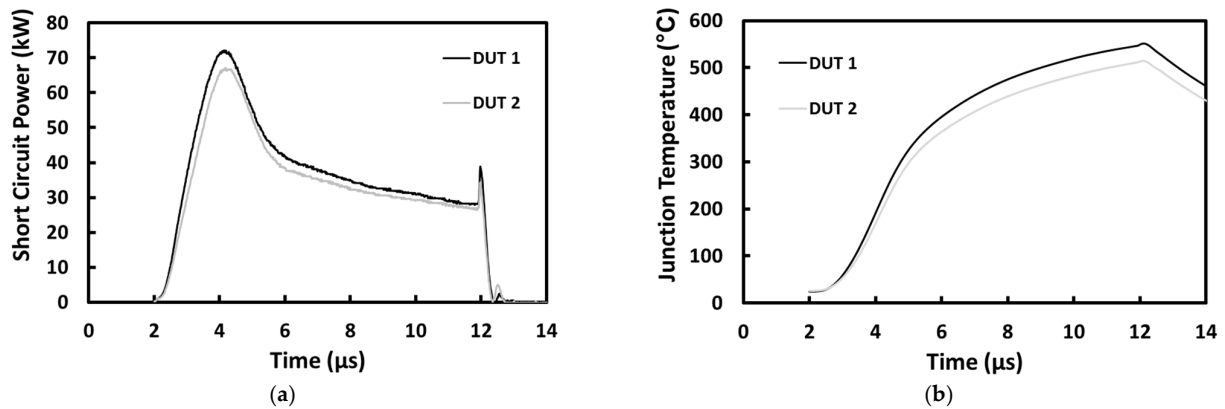
The combined BTI and SC measurements were repeated at a case temperature of 150 °C for different stress times to investigate the impact of temperature on BTI and SC current. The results are shown in Figure 16b. Comparing the SC measurements (after BTI stress) in Figure 16a,b shows that temperature increases the extent of  $V_{TH}$  increase leading to SC charge reduction. All devices exhibit increased effect of  $V_{TH}$  shift as temperature is increased; however, the change is not uniform. Device A shows a SC charge that reduces by 1.5% for  $V_{GS}$  stress at 25 °C to 8% at 150 °C. Device B shows a SC charge that reduces by 1% for  $V_{GS}$  stress at 25 °C to 4% at 150 °C. Device C shows a SC charge that reduces by 2% for  $V_{GS}$  stress at 25 °C to 3% at 150 °C. These measurements were also performed on the Si IGBT, and as can be seen from the Figures, there has been no change in the SC charge due to  $V_{GE}$  stress or temperature.



**Figure 16.** Impact of BTI on SC charge for 1.2 kV SiC MOSFETs and Si IGBT at a case temperature of (a) 25 °C, and (b) 150 °C. Impact of  $V_{GS}$  stress time is apparent for SiC MOSFETs.

#### 4. Datasheet-Based Thermal Modeling and Finite Element Electrothermal Simulations of Short Circuits

Simulations have been performed to investigate the impact of  $V_{TH}$  mismatch on the junction temperatures of the power devices. The goal of the datasheet-based thermal modeling here is to use experimental SC measurements combined with a datasheet-provided thermal network to estimate the device junction temperature. First, the measured short circuit power from the experimental results is fed into the 5-layer Cauer thermal network provided by the manufacturer, and the resulting junction temperatures are evaluated. The devices are mounted in different heatsinks (as shown in Figure 1b); hence, the mutual thermal impedance can be neglected. Figure 17a shows the measured short circuit power for the parallel DUTs, while Figure 17b shows the simulated junction temperatures. Since experimental measurements (shown in Figure 17a) are used for evaluating junction temperature, the temperature dependencies of the device parameters and therefore self-heating, are already considered. Additionally, the transient thermal impedance characteristics provided on the datasheet is experimentally derived, the temperature dependencies of the thermal resistance and capacitances are accounted for. Figure 17b shows that there is a 6.8% difference in the peak junction temperatures between the two devices. Since the thermal simulations assume uniform temperature distribution in the power device, the temperatures in Figure 17b are likely underestimated values of the temperature hot-spots within the chip.



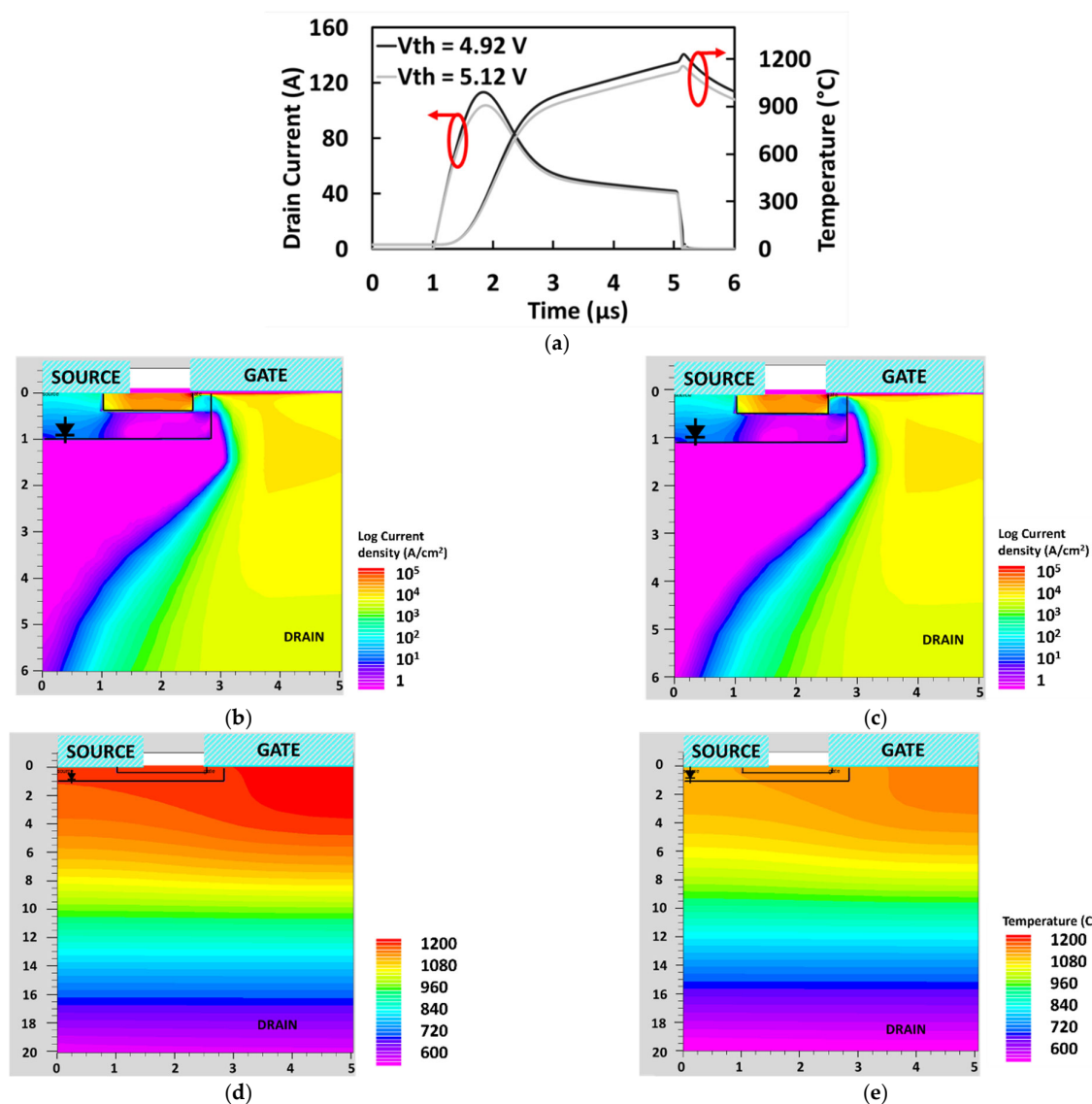
**Figure 17.** Measured SC power and simulated temperature for the parallel 1.2 kV SiC MOSFETs with 25% difference in  $V_{TH}$ : (a) measured SC power; (b) simulated temperature.

To investigate the impact of  $V_{TH}$  shift on the internal current and temperature distribution of SiC MOSFETs, finite element simulations of SiC MOSFETs under short-circuit conditions have been performed in ATLAS (from Silvaco). For this investigation, a 2D model for a SiC MOSFET cell was simulated with the drift layer thickness and doping designed to achieve the required breakdown voltage. The thermal boundary conditions were defined in the simulation by specifying a lumped thermal resistance and capacitance chosen to replicate the thermal characteristics of the device according to the datasheet. The simulation solves the drift–diffusion equations fully coupled with the heat flow equation to yield a thermal map identifying the hot-spot location within the MOSFET cell. The temperature dependency of all semiconductor parameters (effective mobility and intrinsic carrier concentration) is accounted for. This 2D model can provide a qualitative insight of the temperature and current distributions within the device. Table 1 shows the parameters used in the finite element model. The threshold voltage of the MOSFET in the simulation is controlled by varying the doping in the current spreading layer. By varying this doping between parallel devices, the electrothermal dynamics of current sharing can be investigated using the simulator.

**Table 1.** Simulation parameters.

Parameter	MOSFET 1	MOSFET 2
Source doping ( $\text{cm}^{-3}$ )	$1 \times 10^{19}$	$1 \times 10^{19}$
Channel length ( $\mu\text{m}$ )	0.2	0.2
Drift thickness ( $\mu\text{m}$ )	8	8
Drift doping ( $\text{cm}^{-3}$ )	$1.5 \times 10^{15}$	$1.5 \times 10^{15}$
Channel doping ( $\text{cm}^{-3}$ )	$1.5 \times 10^{17}$	$1.5 \times 10^{17}$
Drain doping ( $\text{cm}^{-3}$ )	$1 \times 10^{19}$	$1 \times 10^{19}$
Oxide thickness (nm)	50	50
Thermal resistance (K/W)	0.39	0.39
Current spreading layer doping ( $\text{cm}^{-3}$ )	$1.5 \times 10^{16}$	$1 \times 10^{16}$

Figure 18a shows the simulated SC current and hot-spot temperature of 2 parallel SiC MOSFETs with 4% difference in  $V_{TH}$ . The hot-spot temperature (shown in Figure 18a) within the device is approximately double that predicted by the compact model in Figure 17b, which uses the manufacturer provided thermal network. Figure 18b,c compares the current density for the simulated parallel devices with 4% difference in  $V_{TH}$ , while Figures 18d and 16e compare the hot-spot temperatures. Higher current density and lattice temperature can be observed in the device with the lower  $V_{TH}$  with a corresponding larger hot-spot area compared to the device with the higher  $V_{TH}$ .



**Figure 18.** Simulated SC current and hot-spot temperature using finite elemental model and 2D plot results taken at 4  $\mu$ s into the short circuit for the SiC MOSFET: (a) simulated SC current and hot-spot temperature; (b) 2D current density plot ( $V_{TH} = 4.92$  V); (c) 2D current density plot ( $V_{TH} = 5.12$  V); (d) 2D temperature contour plot of the SiC MOSFET ( $V_{TH} = 4.92$  V); (e) 2D temperature contour plot of the SiC MOSFET ( $V_{TH} = 5.12$  V).

## 5. Conclusions

This paper investigated the impact of variations in the threshold voltage, initial junction temperature and gate resistance on the sharing of SC current in parallel power devices. The results show that variations in  $V_{TH}$  are most critical to SC current sharing. The SC current per device increases with the number of parallel devices due to the reduction of the total inductance across the voltage source. Hence, current sharing in large current capacity power modules is more critical as the number of parallel devices increases.  $V_{TH}$  shift from BTI in SiC MOSFETs is well understood to be a more challenging reliability concern compared to silicon devices. This paper shows that  $V_{GS}$  stresses on the gate oxide of SiC MOSFETs at the rated  $V_{GS}$  is capable of causing a change in the peak SC current and SC charge due to  $V_{TH}$  shift. Subsequent measurements of SC currents 15 min after the stress have shown a reversion to the pre-stress SC characteristics, thereby indicating a release of the trapped charge and a restoration of the pre-stress  $V_{TH}$ . The change in the peak SC current and SC charge is proportional to the  $V_{GS}$  stress duration and temperature, thereby

indicating that the time constants of the trapped charge have a negative temperature coefficient. Electrothermal simulations have shown that a 25% difference in  $V_{TH}$  between parallel connected SiC MOSFETs under SC can result in 6.8% difference in the peak junction temperature. Finite element simulations of SiC MOSFETs under short-circuit conditions show that the hot-spot temperatures are at least twice those predicted from manufacturer provided thermal models. The issue of  $V_{TH}$  mismatch and BTI is shown to be assessed in SiC MOSFETs, and an experimental methodology has been presented to quantify the effects.

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